6' cont'd electrode being doped at a second concentration higher than said first concentration.

REMARKS

Claims 1, 2, 5 and 6 have been cancelled. New claims 9 -18 have been added. Claims 9 - 18 remain in the application. As presently amended, the application includes two independent and a total of 10 claims. Applicant has previously paid for three independent and a total of 20 claims. No new fees are owning.

It is an object of applicant's invention to create MOS transistors having different operating voltages on a single substrate. The prior art, as exemplified by Tigelaar et al., believed that it was necessary to vary the thickness of the gate oxide under the gate electrode to achieve this result. However, as described at pages 2 - 3 of applicant's specification, this required additional process steps and increased the cost of the transistor fabrication process.

Applicant has recognized that this desired result (forming MOS transistors with different operating voltages) could be achieved without changing the thickness of the gate oxides. Rather, the applicant has recognized that this result can be achieved by varying the impurity concentration in the gate electrodes themselves. By providing a lower concentration of impurities in the gate electrode, applicant's invention sets up a depletion layer which operates as an insulating layer thereby reducing the electric filed applied to the gate insulating film and increasing the operating

voltage of the transistor when a reverse bias is applied to the gate electrode. See the paragraph bridging pages 20 – 21 of applicant's specification.

Applicant has further recognized that this desirable result can be enhanced by forming a gate oxide layer under the gate electrode which is thicker at its edges than at its middle portion.

The art of record is silent as to the foregoing result. As noted above, Tigelaar et al, clearly teaches that the desired result of providing MOS transistors with different operating voltages should be achieved by varying the thickness of the gate oxide, not be varying the concentration of impurities in the gate electrode.

This deficiency of Tigelaar et al is not overcome by Kuroda. Initially, Kuroda deals with variations in the threshold level of various transistors, not the operating level thereof. In any event, Kuroda teaches that this variation should be achieved by varying the concentration of impurities in the drain and source regions, not in the gate electrodes as required by applicant's claims.

For all of the foregoing reasons, it is submitted that applicant's claims are neither anticipated nor made obvious by the art of record. Reconsideration and allowance of the application are earnestly solicited.

Attached hereto is a marked-up version of the changes made to the specification, abstract and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

In the Claims:

9. (New) A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer onto said gate oxide layer;

patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;

doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said gate electrodes being doped at a first concentration; and

doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration.

10. (New) The method of claim 9, wherein said doping steps comprise implanting ions of an impurity in said first and second active regions and said first and second gate electrodes.

11. (New) The method of claim 9, wherein said lower concentration of impurities in said first gate electrode causes the creation of a depletion layer in said first gate electrode when a driving voltage is applied thereto.

12. (New) The method of claim 9, wherein said first active region and said first gate electrode are doped simultaneously.

13. (New) The method of claim 12, wherein said second active region and said second gate electrode are doped simultaneously.

14. (New) The method of claim 12. further including the step of forming a gate oxide under each of said gate electrodes.

15. (New) The method of claim 14, wherein both of said gate oxides are the same thickness.

16. (New) The method of claim 15, wherein both of said gate oxides have a shape wherein they are thicker at side edges of said gate electrodes than at the center thereof.

17. (New) The method of claim 16, further including oxidizing said side walls of said gate electrodes, said gate oxides under each of said gate electrodes being formed while said side walls are oxidized.

18. (New) A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer onto said gate oxide layer;

patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;

oxidizing sidewalls of said first and second gate electrodes to form an oxide film under said gate electrodes, said oxide film being thicker at said side walls than at a center portion of said gate electrodes;

doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said gate electrodes being doped at a first concentration; and

doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration.

APPENDIX B
"Clean" Version Without Amended/New Indications
37 C.F.R. § 1.121(b)(1)(iii) AND (c)(3)

CLAIMS:

Cancel claims1,2,5 and 6.

9. A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer onto said gate oxide layer;

patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;

doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said gate electrodes being doped at a first concentration; and

doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration.

10. The method of claim 9, wherein said doping steps comprise implanting ions of an impurity in said first and second active regions and said first and second gate electrodes.

11. The method of claim 9, wherein said lower concentration of impurities in said first gate electrode causes the creation of a depletion layer in said first gate electrode when a driving voltage is applied thereto.

12. The method of claim 9, wherein said first active region and said first gate electrode are doped simultaneously.

13. The method of claim 12, wherein said second active region and said second gate electrode are doped simultaneously.

14. The method of claim 12. further including the step of forming a gate oxide under each of said gate electrodes.

15. The method of claim 14, wherein both of said gate oxides are the same thickness.

16. The method of claim 15, wherein both of said gate oxides have a shape wherein they are thicker at side edges of said gate electrodes than at the center thereof.

17. The method of claim 16, further including oxidizing said side walls of said gate electrodes, said gate oxides under each of said gate electrodes being formed while said side walls are oxidized.

18. A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

providing a semiconductor substrate having at least first and second active regions of a first conductivity type;

forming a gate oxide layer having a first thickness onto at least said first and second active regions;

forming an electrode layer onto said gate oxide layer;

patterning said electrode layer to form first and second gate electrodes onto said first and second active regions, respectively;

oxidizing sidewalls of said first and second gate electrodes to form an oxide film under said gate electrodes, said oxide film being thicker at said side walls than at a center portion of said gate electrodes;

doping said first active region and said first gate electrode with an impurity of a second conductivity type which is opposite to said first conductivity type to form a first transistor driven at a first voltage level, said gate electrodes being doped at a first concentration; and

doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration.